Problem 4.

LIBRARY ieee ;

USE ieee.std logic 1164.all ;

ENTITY dec3to8 IS

PORT ( w : IN STD LOGIC VECTOR(2 DOWNTO 0) ;

En : IN STD LOGIC ;

y : OUT STD LOGIC VECTOR(0 TO 7) ) ;

END dec3to8 ;

ARCHITECTURE Behavior OF dec3to8 IS

BEGIN

PROCESS ( w, En )

BEGIN

IF En = ’1’ THEN

CASE w IS

WHEN ”001” =>

y <= ”00000000” ;

WHEN ”110” =>

y <= ”00000000” ;

WHEN OTHERS =>

y <= ”0001” ;

END CASE ;

ELSE

y <= ”0000” ;

END IF ;

END PROCESS ;

END Behavior ;

Problem 8.

library IEEE;

use IEEE.STD\_LOGIC\_1164.all;

use ieee.numeric\_std.all;

entity priority\_encoder\_8\_3 is

port(

A : in STD\_LOGIC\_VECTOR(7 downto 0);

Z : out STD\_LOGIC\_VECTOR(2 downto 0)

);

end priority\_encoder\_8\_3;

architecture priority\_enc\_arc of priority\_encoder\_8\_3 is

begin

Z <= "000" when A(7)='1' else

"001" when A(6)='1'else

"010" when A(5)='1' else

"011" when A(4)='1' else

"100" when A(3)='1' else

"101" when A(2)='1' else

"110" when A(1)='1' else

"111" when A(0)='1';

end priority\_enc\_arc

Problem 9

library IEEE;

use IEEE.STD\_LOGIC\_1164.all;

use ieee.numeric\_std.all;

entity priority\_encoder\_8\_3 is

port(

A : in STD\_LOGIC\_VECTOR(7 downto 0);

Z : out STD\_LOGIC\_VECTOR(2 downto 0)

);

end priority\_encoder\_8\_3;

architecture priority\_enc\_arc of priority\_encoder\_8\_3 is

begin

process (A)

begin

if A(0) = '1' then

Z <= "111";

elsif A(1)= '1' then

Z <= "110";

elsif A(2)='1' then

Z <= "110";

elsif A(3)='1' then

Z <= "100";

elsif A(4)='1' then

Z <= "011";

elsif A(5)='1' then

Z <= "010";

elsif A(6)='1' then

Z <= "001";

elsif A(7)='1' then

Z <= "000";

else

Z <= "000";

end if;

end process;

end priority\_enc\_arc;

